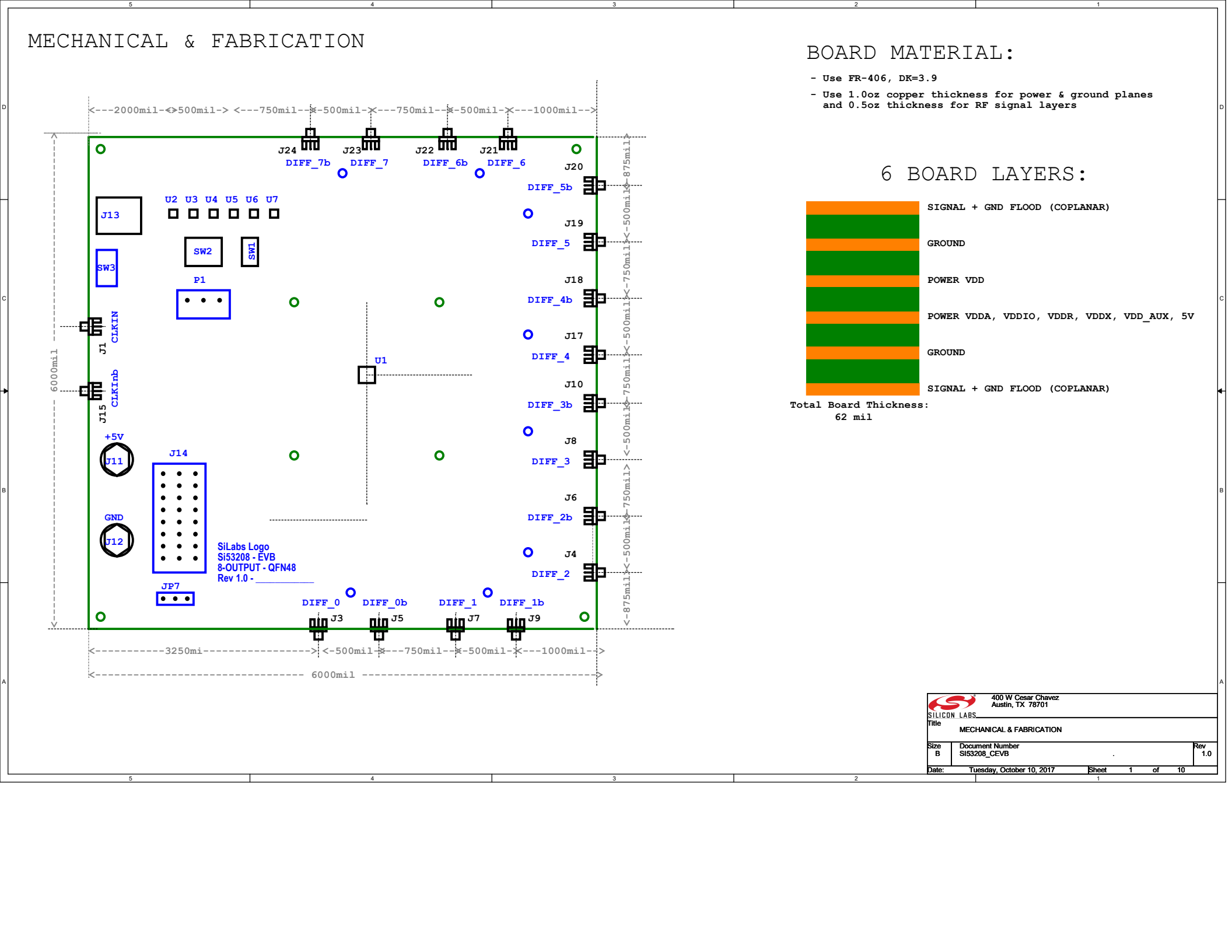


MECHANICAL & FABRICATION

[illegible]

- ## MECHANICAL & FABRICATION
-

MECHANICAL & FABRICATION



MECHANICAL & FABRICATION

SiLabs Logo
SI53208 - EVB
8-OUTPUT - QFN48
Rev 1.0 -

BOARD MATERIAL:

- Use FR-406, DK=3.9
- Use 1.0oz copper thickness for power & ground planes and 0.5oz thickness for RF signal layers

6 BOARD LAYERS:

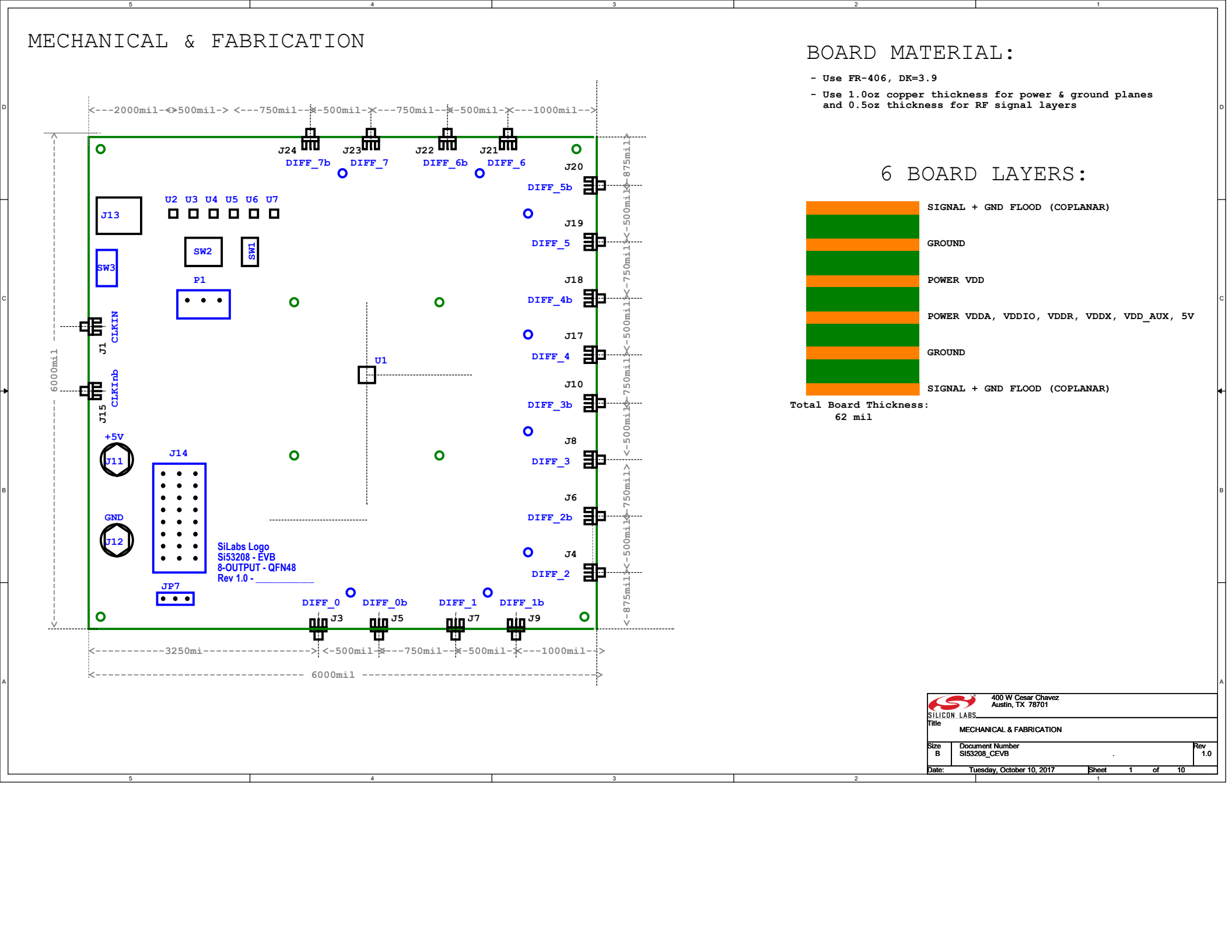
Total Board Thickness:
62 mil

SILICON LABS.
400 W Cesar Chavez
Austin, TX 78701

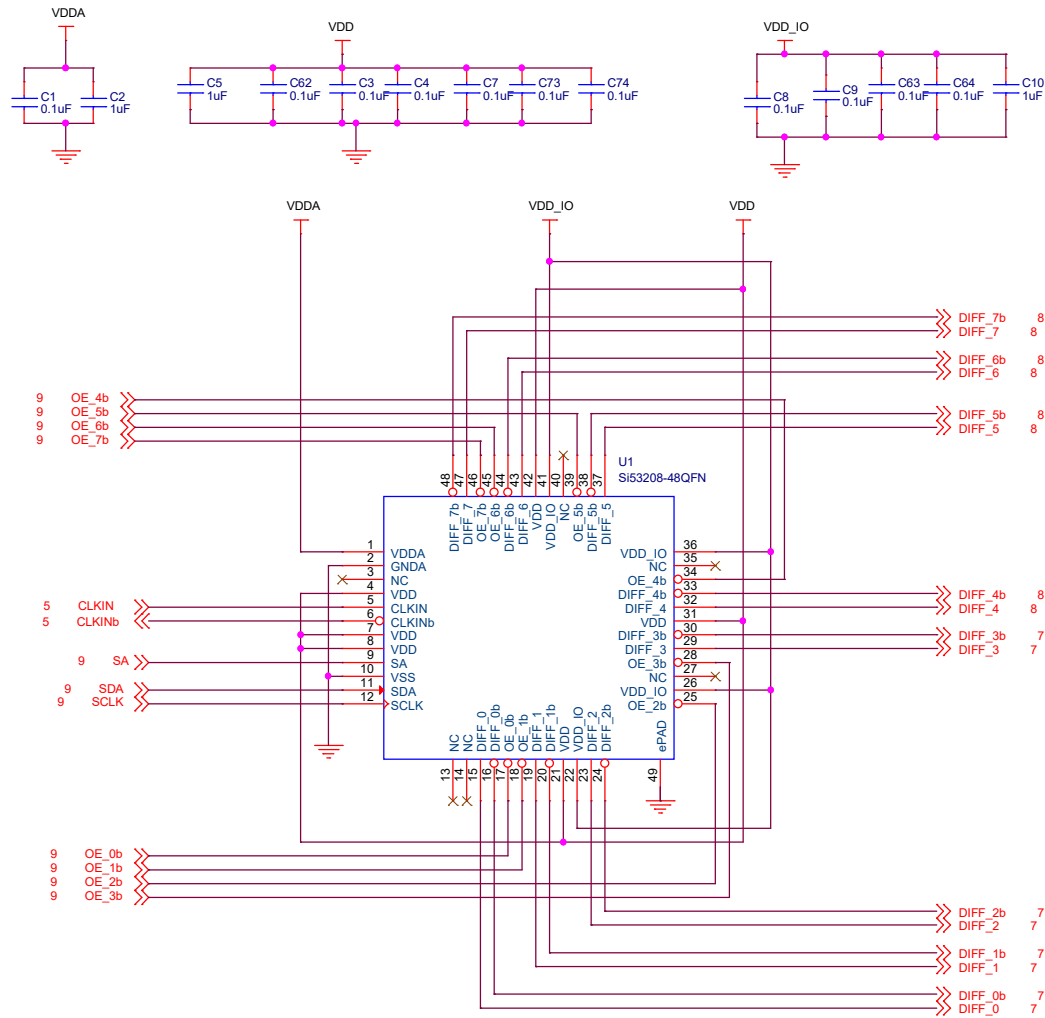
Title
MECHANICAL & FABRICATION

Size B Document Number SI53208_CEVb Rev 1.0

Date: Tuesday, October 10, 2017 Sheet 1 of 10



DUT CONNECTIONS

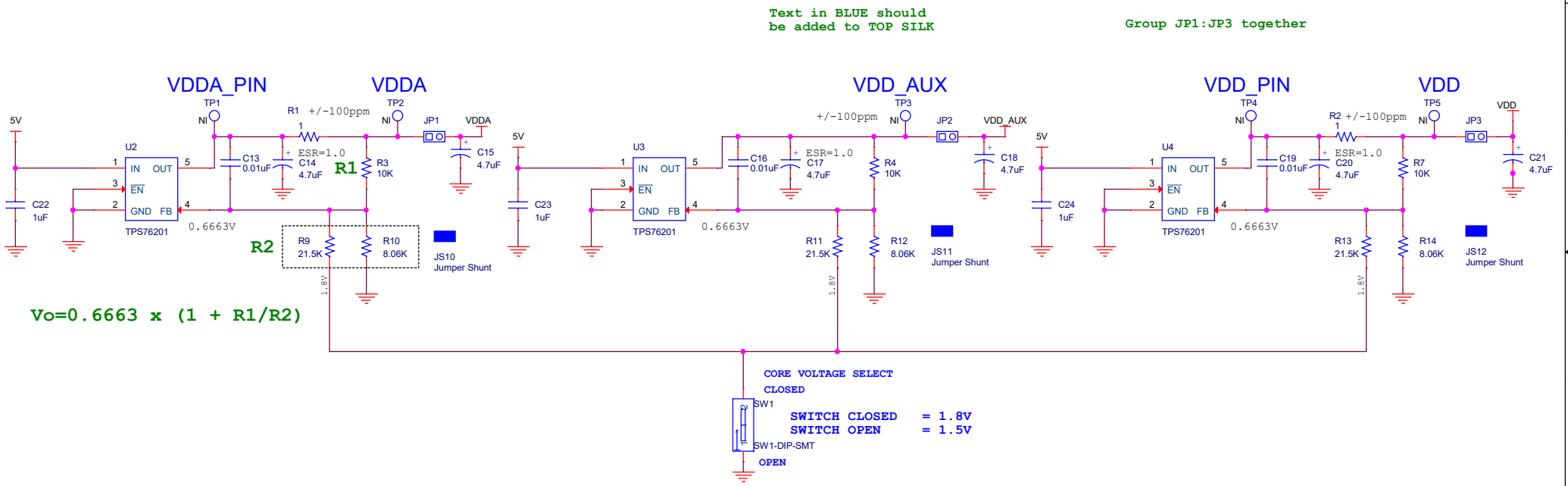


Place as many vias between copper flood for ePAD and ground as possible!



		400 W Cesar Chavez Austin, TX 78701	
SILICON LABS.		Title	
DUT Connections		Rev	
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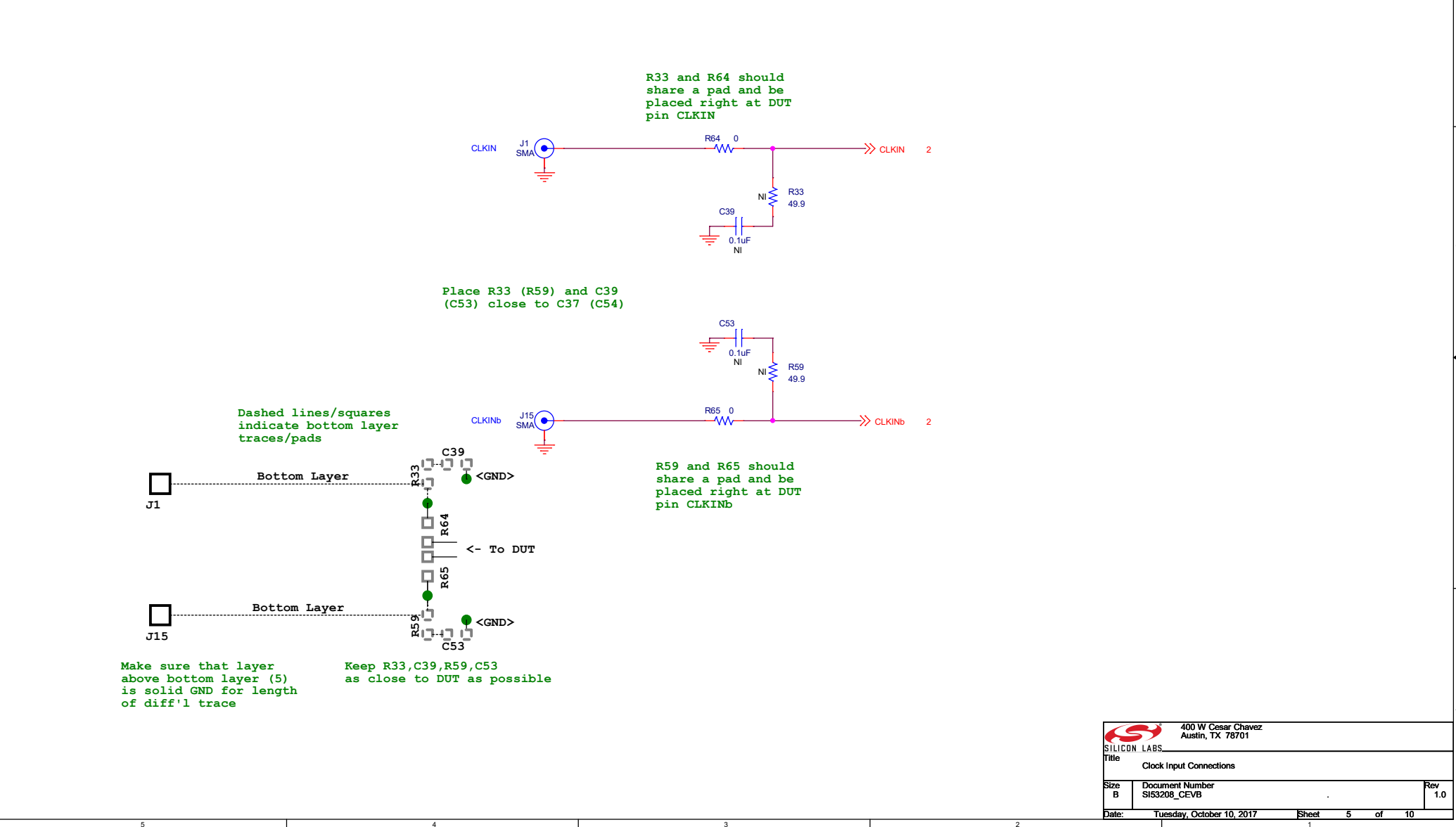
100 mA Adjustable Voltage Regulator



Identify Pin1 of all jumpers and IC's!

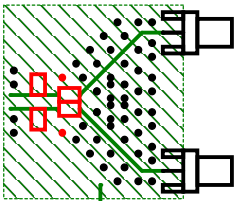
		400 W Cesar Chavez Austin, TX 78701	
SILICON LABS Title Other Voltage Regulators			
Size B	Document Number SI53208-CEVB		Rev 1.0
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Clock Input Connections



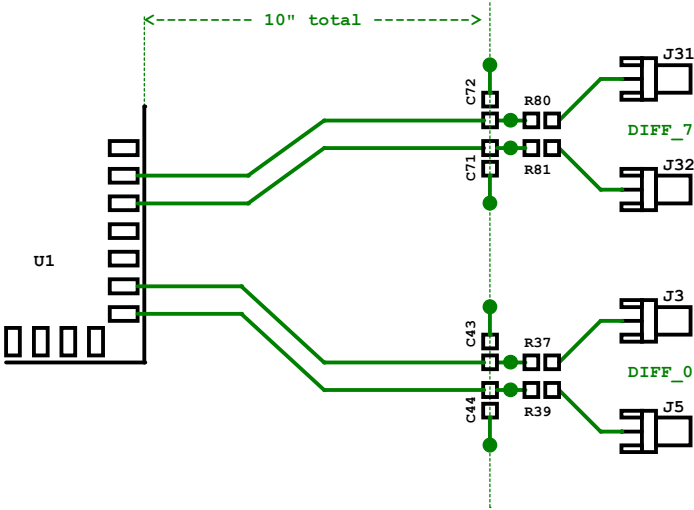
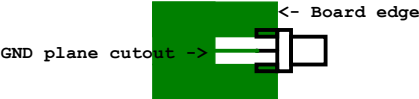
OUTPUT CONNECTIONS, PART 1

Flood top and bottom layers with copper as shown



A sufficient number of via holes connected to ground should be used around all input/output traces!

SMA FOOTPRINT NOTE:
Make sure pad for center pin on SMA matches exactly the actual width of the center pin in order to improve performance

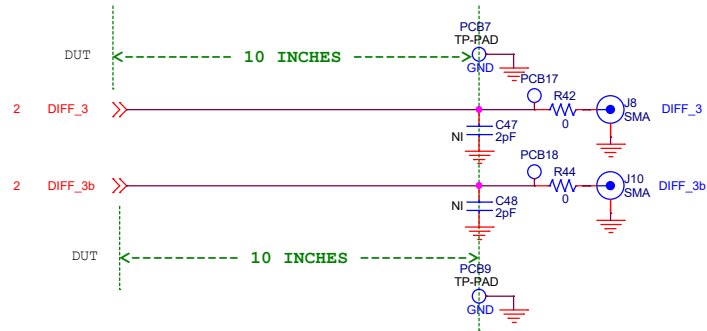
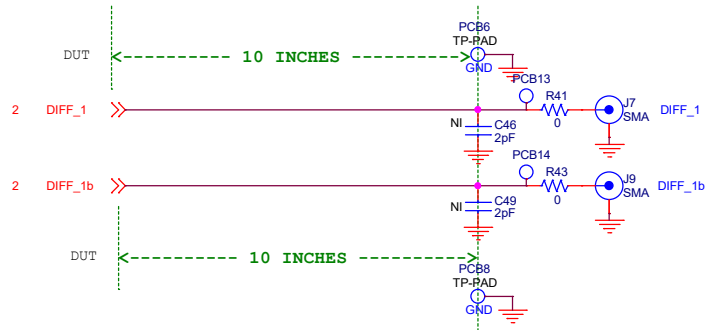
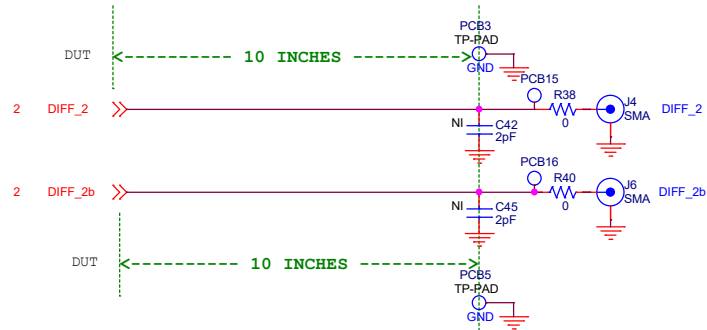
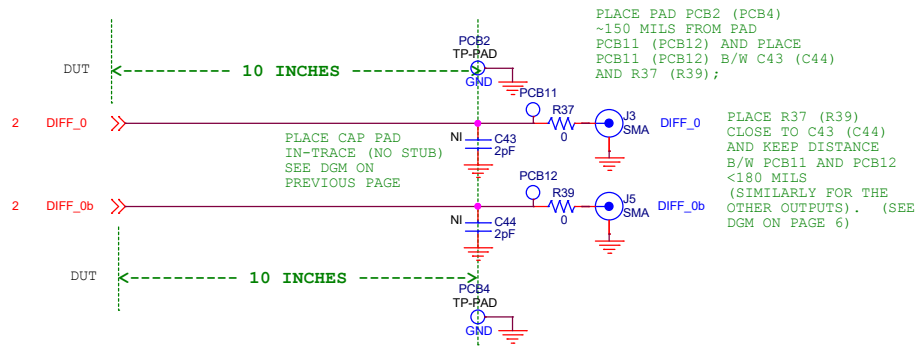


OUTPUT SIGNALS LAYOUT NOTES - APPLIES TO THIS PAGE AND NEXT PAGE AS WELL!
(Refer to image on left):

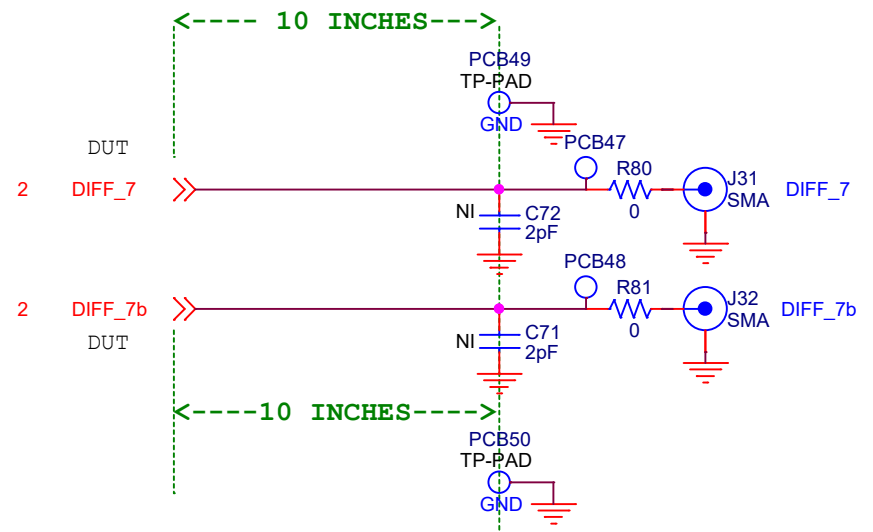
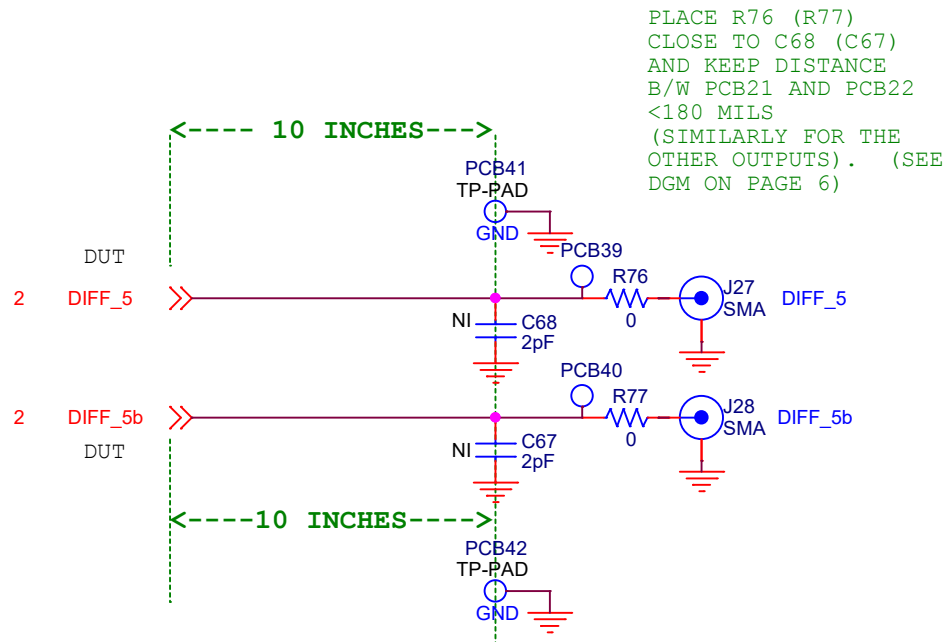
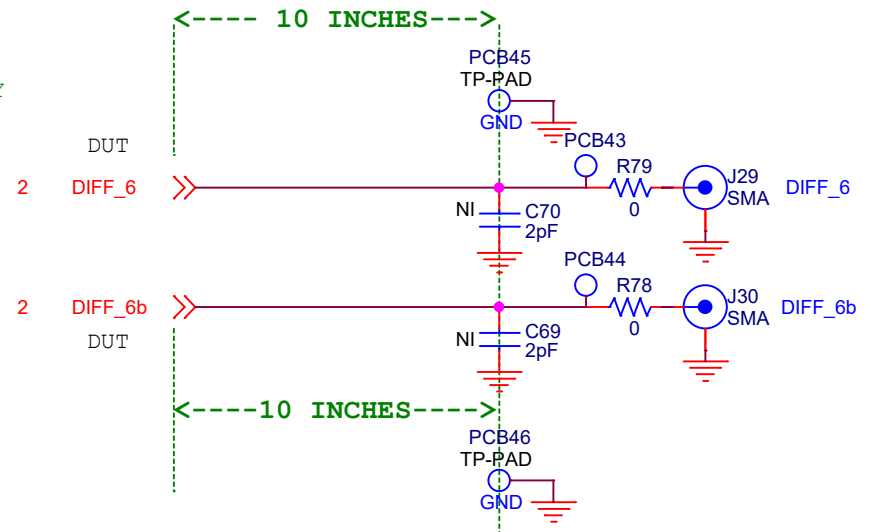
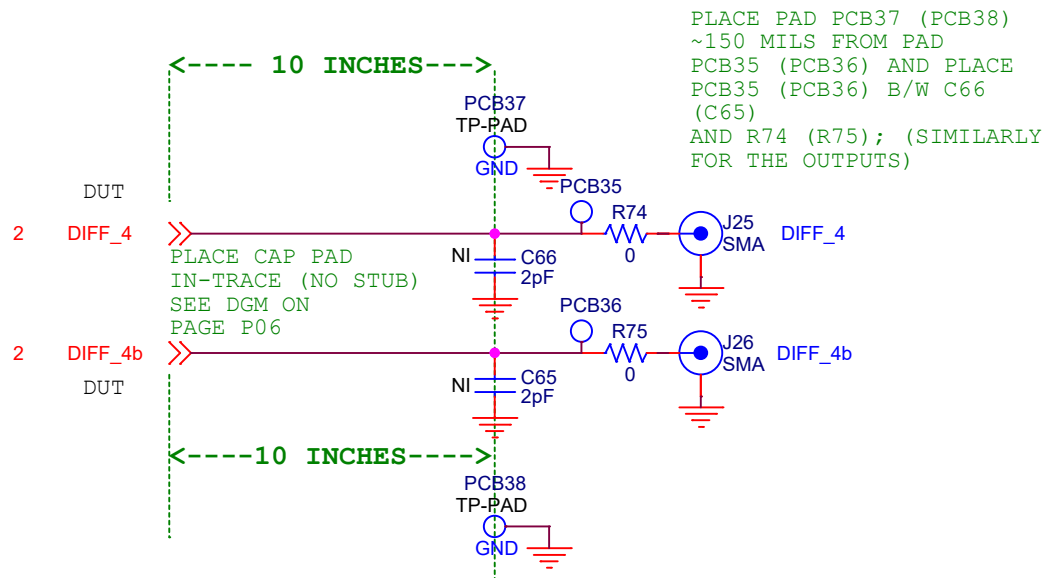
- ROUTING: route each differential pair loosely coupled. Serpentine to length and preserve symmetry on diff. pair. Keep distance b/w serpentine traces at least 5w apart and use arcs rather than 45's
- IMPEDANCE: all traces to have 50 ohms of controlled impedance
- In order to reduce capacitance please cut-out ground planes underneath the microstrip launches on the SMA connectors as needed
- GEOMETRY: maintain the trace symmetry across all output differential pairs
- TOPOLOGY: use microstrip for all traces
- COMPONENT PLACEMENT:
 - Separate each pair of SMA connectors by 500 mils between them (center to center), and 750 mils pair to pair)

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SILICON LABS.		Title	
		Output Connections	
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OUTPUT CONNECTIONS



OUTPUT CONNECTIONS



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SILICON LABS

Title

Outputs 4-7

Size
A

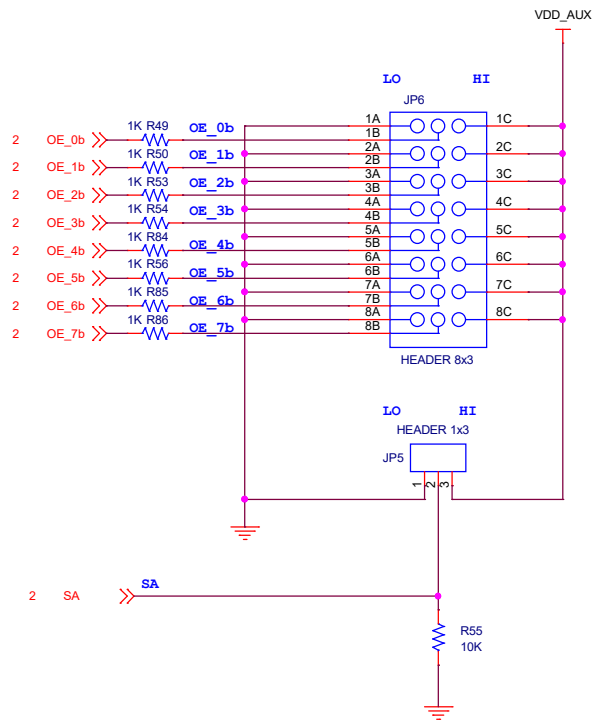
Document Number
SI53208_CEVb

Rev
1.0

Date: Tuesday, October 10, 2017

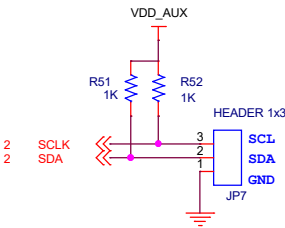
Sheet 8 of 10

DC Inputs/I2C Access



	LO	NONE	HI
OE_0b	EN	EN	DSBL
OE_1b	EN	EN	DSBL
OE_2b	EN	EN	DSBL
OE_3b	EN	EN	DSBL
OE_4b	EN	EN	DSBL
OE_5b	EN	EN	DSBL
OE_6b	EN	EN	DSBL
OE_7b	EN	EN	DSBL

	LO	NONE	HI
SA, Address Select	0	0	1



- JS2 Jumper Shunt
- JS3 Jumper Shunt
- JS4 Jumper Shunt
- JS5 Jumper Shunt
- JS6 Jumper Shunt
- JS7 Jumper Shunt
- JS8 Jumper Shunt
- JS9 Jumper Shunt
- JS16 Jumper Shunt

5	4	3	2	1
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